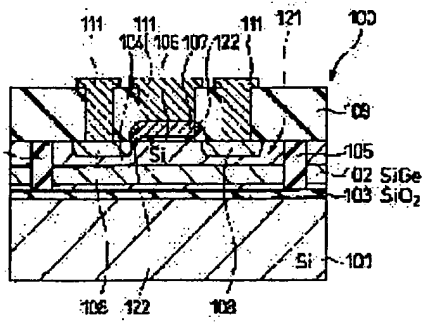
B51

2000-031491 HITACHI Sugii

R DEVICE, ITS MANUFACTURE,
R SUBSTRATE AND ITS MANUFACTURE



PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2000-031491**

(43)Date of publication of application : **28.01.2000**

(51)Int.Cl. **H01L 29/786**
H01L 29/78
H01L 29/778
H01L 21/338
H01L 29/812

(21)Application number : **10-197911**

(22)Date of filing : **14.07.1998**

(71)Applicant : **HITACHI LTD**

(72)Inventor : **SUGII NOBUYUKI**
NAKAGAWA KIYOKAZU
YAMAGUCHI SHINYA
MIYAO MASANOBU

(54) **SEMICONDUCTOR DEVICE, ITS MANUFACTURE, SEMICONDUCTOR SUBSTRATE AND ITS MANUFACTURE**

(57)Abstract:

PROBLEM TO BE SOLVED: To perform acceleration or the like by setting a strain application layer made of a mixed crystal semiconductor layer to the thickness of a specific range, and reducing the thickness of an Si layer between SiGe strain application layer and an SiO2 insulating layer at most to the thickness of the SiGe strain application layer, thereby setting the thickness of the strain channel layer to the critical thickness of Si of a specific value or less on the SiGe.

SOLUTION: In the semiconductor device 100, an SiGe strain application layer 102 made of an SiGe ($0 \leq x \leq 1$) and a strain Si channel layer 104 are sequentially laminated and grown on an upper surface of an Si substrate 101, and a structure having an SiO2 insulating layer 103 therein is formed at a surface layer of the substrate 101. The layer 102 of the device 10 is formed in a thickness of about 50 to 200 nm, and the thickness of the Si layer between the layer 102 and the layer 103 is set to the thickness of less of the SiGe strain application layer. Further, the thickness of the layer 104 is set to a power of about (3-2x) times of 10 as a critical thickness nm in which Si is strain grown on the SiGe.

Best Available Copy

SEMICONDUCTOR DEVICE, ITS MANUFACTURE, SEMICONDUCTOR SUBSTRATE AND ITS MANUFACTURE

2000-031491 HITACHI Sugii

CLAIMS

[Claim(s)]

[Claim 1] SiO2 insulating layer which is formed in Si substrate and formed inside the principal plane of the aforementioned Si substrate. It consists of a mixed-crystal semiconductor layer prepared on the principal plane of the aforementioned Si substrate, is distorted, and is an impression layer. It consists of an Si layer prepared on the aforementioned distortion impression layer, is distorted, and is a channel layer. The diffusion field of the couple which is prepared in the aforementioned distortion channel layer and constitutes a source field or a drain field. The field effect transistor constituted by the gate electrode prepared through a gate insulator layer on the distortion channel layer between the diffusion fields of the aforementioned couple. Are the semiconductor device equipped with the above and the aforementioned distortion impression layer consists of Si1-xGex (0<=x<=1). The aforementioned distortion impression layer becomes the thickness of about 50-200nm, and Si layer thickness between the aforementioned Si1-xGex distortion impression layer and the SiO2 aforementioned insulating layer turns into thickness below the aforementioned Si1-xGex distortion impression layer. The aforementioned distortion channel layer thickness is characterized by having become below the ** (3-2x) nm grade of 10.

[Claim 2] The semiconductor device characterized by providing the following. It is formed in Si substrate, and it consists of a mixed-crystal semiconductor layer prepared on the principal plane of the aforementioned Si substrate, is distorted, and is an impression layer. SiO2 insulating layer prepared in the aforementioned Si substrate so that the upper surface may extend along with the aforementioned distortion impression layer in contact with the undersurface of the aforementioned distortion impression layer. It consists of an Si layer prepared on the aforementioned distortion impression layer, is distorted, and is a channel layer. The field effect transistor constituted by the gate electrode prepared through a gate insulator layer on the distortion channel layer between the diffusion field of the couple which is prepared in the aforementioned distortion channel layer and constitutes a source field or a drain field, and the diffusion field of the aforementioned couple.

[Claim 3] It is the semiconductor device according to claim 2 characterized by for the aforementioned distortion impression layer consisting of Si1-xGex (0<=x<=1), for the aforementioned distortion impression layer becoming the thickness of 50-200nm, and the aforementioned distortion channel layer thickness having become below the ** (3-2x) nm grade of 10.

[Claim 4] A semiconductor device given in any 1 term of the claim 1 characterized by forming a spacer layer, the carrier supply layer by which the conductivity-type determination impurity was doped, and a cap layer one by one on the aforementioned distortion channel layer, and constituting the modulation dope type field effect transistor, or a claim 3.

[Claim 5] The manufacture method of a semiconductor device of it being distorted, and having a channel layer and having the field effect transistor which consists of an Si layer between the source fields and drain fields which are characterized by providing the following, and which it was formed in Si substrate and established in the aforementioned Si substrate and which is constituted by preparing a gate electrode through a gate insulator layer on the distortion channel layer between the aforementioned source field and a drain field. The process which becomes the principal plane of the aforementioned Si substrate from a mixed-crystal semiconductor layer and which is distorted and forms an impression layer. The process which anneals while pouring in oxygen ion from the front face of the aforementioned distortion impression layer, and forms SiO2 insulating layer in the aforementioned Si substrate. The process which forms the aforementioned distortion channel layer on the aforementioned distortion impression layer. The process which forms an isolation insulating region and forms an element formation field in the principal plane side of the aforementioned Si substrate, and the process which forms the diffusion field which constitutes the aforementioned gate electrode and a source field, and a drain field in the aforementioned element formation field.

[Claim 6] The manufacture method of the semiconductor device according to claim 5 characterized by forming so that pouring of the aforementioned oxygen ion and the processing conditions of annealing may be chosen and the surface portion of the aforementioned Si substrate may remain between the aforementioned distortion impression layer and the SiO2 aforementioned insulating layer.

[Claim 7] The manufacture method of the semiconductor device according to claim 5 characterized by

forming so that pouring of the aforementioned oxygen ion and the processing conditions of annealing may be chosen and the upper surface of the SiO2 aforementioned insulating layer may be in agreement with the inferior surface of tongue of the aforementioned distortion impression layer.
[Claim 8] The manufacture method of a semiconductor device given in any 1 term of the claim 5 characterized by forming a spacer layer, the delta carrier supply layer by which the conductivity-type determination impurity was doped, and a cap layer one by one, and forming a modulation dope type field effect transistor on the aforementioned distortion channel layer, or a claim 7.
[Claim 9] It is the manufacture method of a semiconductor device given in any 1 term of the claim 5 characterized by forming the aforementioned distortion impression layer in the thickness of 50-200nm, and forming the aforementioned distortion channel layer thickness below in the ** (3-2x) nm grade of 10, or a claim 8.
[Claim 10] The semiconductor substrate which consists of SiO2 insulating layer formed in the principal plane of Si substrate and the aforementioned Si substrate of annealing processing of the oxygen ion poured in from the front face of the mixed-crystal semiconductor layer by which growth formation was carried out, and the aforementioned mixed-crystal semiconductor layer.
[Claim 11] The semiconductor substrate according to claim 10 characterized by Si layer which constitutes Si substrate below the aforementioned mixed-crystal semiconductor layer thickness existing between the SiO2 aforementioned insulating layer and the aforementioned mixed-crystal semiconductor layer.
[Claim 12] The semiconductor substrate according to claim 10 characterized by the upper surface of the SiO2 aforementioned insulating layer being in agreement with the inferior surface of tongue of the aforementioned mixed-crystal semiconductor layer.
[Claim 13] The aforementioned mixed-crystal semiconductor layer thickness is a semiconductor substrate given in any 1 term of the claim 10 characterized by being 50-200nm, or a claim 12.
[Claim 14] The aforementioned mixed-crystal semiconductor layer is a semiconductor substrate given in any 1 term of the claim 10 characterized by consisting of Si1-xGex (0<=x<=1), or a claim 13.
[Claim 15] The manufacture method of the semiconductor substrate which is the manufacture method of an Si substrate given in any 1 term of the aforementioned claim 10 or a claim 14, and is characterized by to have the process which pours in oxygen ion so that the peak of a pouring distribution in the aforementioned Si substrate may be located in the principal plane of the aforementioned Si substrate from the process which carries out growth formation of the mixed-crystal semiconductor layer, and the front face of the aforementioned mixed-crystal semiconductor layer, and the process which anneal the aforementioned Si substrate and form the

---

[Translation done.]

SEMICONDUCTOR DEVICE, ITS MANUFACTURE, SEMICONDUCTOR SUBSTRATE AND ITS MANUFACTURE

2000-031491 HITACHI Sugii

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention is applied to the manufacturing technology of the semiconductor device containing a SiGe hetero structure transistor about the manufacture method of the manufacture method of a semiconductor device and a semiconductor device, a semiconductor substrate, and a semiconductor substrate, and relates to effective technology.
[0002]
[Description of the Prior Art] In connection with the densification of an integrated circuit, the size reduction and the improvement in speed in Si field-effect transistor serve as pressing need. On the other hand, development of the high-speed low-power transistor for communication is also desired strongly.
[0003] it is distorted and the thing which was made to impress distortion to Si channel and which boil Si (hetero structure) transistor markedly compared with the conventional Si field-effect transistor, and can accelerate is suggested (M. V.Fischetti and S:E.Laux:J.Appl.Phys.80 (1996) 2234)
[0004] In the hetero structure transistor formed on Si substrate, in order to give distortion to a channel layer, it is necessary to prepare the buffer layer (distortion impression layer) from which this and a lattice constant differ in the lower part of a channel layer. Although Si1-xGex mixed crystal (0<=x<=1) was conventionally used as a buffer layer, realization of the high mobility transistor which needs to carry out the laminating of the buffer layer with a thickness of 1 microns or more, has a bad influence on the transport properties of a channel layer for aggravation of the problem which transposition penetrates to the buffer-layer upper part, or surface roughness, and has desired electronic transport properties was difficult.
[0005] Moreover, it is related with the transistor (field effect transistor) using Si and germanium. EKUSUTENDEDO Abstract OBU 1993 International Conference ON Solid state Device and -- MATERIARUZU MAKUHARI, 1993, The 201st page A page to the 203rd () [Extended] It is discussed by Abstravts of the 1993 International Conference on Solid State Devices and Materials and Makuhari(1993) pp.201-203.
[0006] The field effect transistor (high mobility transistor) indicated by this reference has the structure of having a SiGe buffer layer on Si substrate, and having Si channel layer and a SiGe layer on this SiGe buffer layer. Moreover, the delta dope layer (electronic supply layer) which consists of a single atomic layer which doped Sb is prepared in the middle of the aforementioned SiGe layer.
[0007] SOI which considered high-speed operation and prepared the silicon layer on the electric insulating plate on the other hand Using a substrate is examined. SOI SIMOX which anneals after injecting oxygen ion into Si substrate, although some methods, such as a lamination substrate, are proposed by the substrate, and forms an oxide layer Promising ** of the method is carried out. SIMOX Using a substrate is distorted only not only in the conventional Si field-effect transistor, and it brings about a big advantage also in production of Si transistor.
[0008] That is, if a SiGe distortion impression layer is formed on a SIMOX substrate, since much transposition occurs in Si layer of the SiO2 and the upper part of those in a substrate, it will become possible to make the dislocation density of a SiGe layer mitigate. However, for reduction of dislocation density, also at the lowest, the thickness of a SiGe layer is 500nm or more need, and is not desirable because of the flat nature on the front face of a film, or productivity.
[0009] Thus, formation of a quality distorted impression layer required for realization of a high-speed SiGe hetero structure quantity mobility transistor (HEMT) with the conventional technology was difficult. In addition, the example which formed the field effect transistor and the high mobility transistor using the SIMOX substrate is indicated by D.KNayak, J.S.Park, J.C.S.Woo, KL.Wang, G.KYabiku, and and KP.MacWilliams International Electron Devices Meeting (IEDM).
[0010]
[Problem(s) to be Solved by the Invention] With the above-mentioned conventional technology, there are problems, such as penetration transposition of a buffer layer, aggravation of front-face nature, or productivity aggravation of a buffer layer, and this obstructed realization of a high-speed SiGe hetero structure quantity mobility transistor.

[0011] The purpose of this invention is by realizing hetero structure with good crystallinity to offer the manufacture method of a semiconductor device excellent in the semiconductor device and productivity which have the hetero structure transistor which can attain improvement in the speed, highly-efficient-izing, and high integration.
[0012] Other purposes of this invention are to offer Si substrate (semiconductor substrate) of hetero structure with good crystallinity. The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.
[0013]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
(1) SiO2 insulating layer which is formed in Si substrate and formed inside the principal plane of the aforementioned Si substrate, It consists of a mixed-crystal semiconductor layer prepared on the principal plane of the aforementioned Si substrate, and is distorted. An impression layer, The diffusion field of the couple which is distorted, is prepared in a channel layer and the aforementioned distortion channel layer, and constitutes a source field or a drain field which consists of an Si layer prepared on the aforementioned distortion impression layer, It is the semiconductor device which has the field effect transistor constituted by the gate electrode prepared through a gate insulator layer on the distortion channel layer between the diffusion fields of the aforementioned couple. The aforementioned distortion impression layer consists of Si1-xGex (0<=x<=1), and the aforementioned distortion impression layer becomes the thickness of about 50-200nm. Si layer thickness between the aforementioned Si1-xGex distortion impression layer and the SiO2 aforementioned insulating layer turns into thickness below the aforementioned Si1-xGex distortion impression layer. The aforementioned distortion channel layer thickness has become below the ** (3-2x) nm grade of 10 that is the critical thickness by which Si distorts and grows on Si1-xGex.
[0014] Such an electric field effect type transistor is manufactured by the following manufacture methods. It is formed in Si substrate. Consist of an Si layer between the source fields and drain fields which were established in the aforementioned Si substrate, and it is distorted to it, and have a channel layer, and a gate insulator layer is minded on the distortion channel layer between the aforementioned source field and a drain field. The process which is the manufacture method of a semiconductor device of having the field effect transistor constituted by preparing a gate electrode, and becomes the principal plane of the aforementioned Si substrate from a mixed-crystal semiconductor layer and which is distorted and forms an impression layer, The process which anneals while pouring in oxygen ion from the front face of the aforementioned distortion impression layer, and forms SiO2 insulating layer in the aforementioned Si substrate, It has the process which forms the aforementioned distortion channel layer on the aforementioned distortion impression layer, the process which forms an isolation insulating region and forms an element formation field in the principal plane side of the aforementioned Si substrate, and the process which forms the diffusion field which constitutes the aforementioned gate electrode and a source field, and a drain field in the aforementioned element formation field. Pouring of the aforementioned oxygen ion and the processing conditions of annealing are chosen, and it forms so that the surface portion of the aforementioned Si substrate may remain between the aforementioned distortion impression layer and the SiO2 aforementioned insulating layer. The aforementioned distortion impression layer is formed in the thickness of 50 - 200 nm, and the aforementioned distortion channel layer thickness is formed below in the ** (3-2x) nm grade of 10.
[0015] (2) In the composition of the aforementioned means (1), it has the structure where the upper surface of the SiO2 aforementioned insulating layer touches the inferior surface of tongue of the aforementioned distortion impression layer. It is formed in Si substrate, and it consists of a mixed-crystal semiconductor layer [an Si1-xGex layer (0<=x<=1)] of the thickness 50 prepared on the principal plane of the aforementioned Si substrate - 200 nm, and is distorted. Namely, an impression layer, SiO2 insulating layer prepared in the aforementioned Si substrate so that the upper surface may extend along with the aforementioned distortion impression layer in contact with the inferior surface of tongue of the aforementioned distortion impression layer, The thickness prepared on the aforementioned distortion impression layer consists of an Si layer below the ** (3-2x) nm grade of 10, and it is distorted. A channel layer, It has the composition of having the field effect transistor constituted by the gate

electrode prepared through a gate insulator layer on the distortion channel layer between the diffusion field of the couple which is prepared in the aforementioned distortion channel layer and constitutes a source field or a drain field, and the diffusion field of the aforementioned couple.
[0016] In the manufacture method by the means of the above (1), such an electric field effect type transistor chooses pouring of the aforementioned oxygen ion, and the processing conditions of annealing, and it forms them so that the upper surface of the SiO2 aforementioned insulating layer may be in agreement with the inferior surface of tongue of the aforementioned distortion impression layer.
[0017] (3) In the aforementioned means (1) or the composition of (2), on the aforementioned distortion channel layer, a spacer layer, the carrier supply layer by which the conductivity-type determination impurity was doped, and a cap layer are formed one by one, and constitute the modulation dope type field effect transistor.
[0018] In the above (1) or the manufacture method by the means of (2), on the aforementioned distortion channel layer, such a modulation dope type field effect transistor forms a spacer layer, the delta carrier supply layer by which the conductivity-type determination impurity was doped, and a cap layer one by one, and forms a modulation dope type field effect transistor.
[0019] (4) The semiconductor substrate which consists of SiO2 insulating layer formed in the principal plane of Si substrate and the aforementioned Si substrate of annealing processing of the oxygen ion poured in from the front face of the mixed-crystal semiconductor layer by which growth formation was carried out, and the aforementioned mixed-crystal semiconductor layer. Between the SiO2 aforementioned insulating layer and the aforementioned mixed-crystal semiconductor layer, Si layer which constitutes Si substrate below the aforementioned mixed-crystal semiconductor layer thickness exists. The aforementioned mixed-crystal semiconductor layer consists of an Si1-xGex layer (0<=x<=1), and the thickness has become 50 - 200 nm.
[0020] Such a semiconductor substrate is manufactured according to the process which pours in oxygen ion so that the peak of a pouring distribution in the aforementioned Si substrate may be located in the principal plane of Si substrate from the process which carries out growth formation of the mixed-crystal semiconductor layer, and the front face of the aforementioned mixed-crystal semiconductor layer, and the process which anneals the aforementioned Si substrate and forms the SiO2 aforementioned insulating layer.
[0021] (5) In the composition of the aforementioned means (1), it has composition whose upper surface of the SiO2 aforementioned insulating layer corresponds with the inferior surface of tongue of the aforementioned mixed-crystal semiconductor layer.
[0022] Although the structure of the (a) field effect transistor becomes the same thing as the field effect transistor manufactured using the SIMOX substrate according to the means of the above (1) As compared with about 500nm or more of a SIMOX substrate, SiGe distortion impression layer thickness is thinly made with about 200nm or less below the half, and, as a result, can form the thin distortion Si channel layer below the ** (3-2x) nm grade of thickness 10 on a SiGe distortion impression layer.
[0023] (b) Since flattening of a SiGe distortion impression layer can be attained and distortion Si channel layer thickness can be made thin below the ** (3-2x) nm grade of 10 with the above (a), the fall of the mobility by reduction of the punch-through current of a field-effect transistor and transition generating into a channel layer can be prevented, and the improvement in a property (improvement in the speed, highly-efficient-izing) of a field effect transistor can be attained.
[0024] (c) With the above (b), flattening of a SiGe distortion impression layer can be attained, thin-shape-izing of a distortion Si channel layer to micro processing becomes possible, and high integration can be attained.
[0025] (d) With the above (a), shortening of the formation time of a SiGe distortion impression layer and a distortion Si channel layer can be aimed at, and reduction of the manufacturing cost of a semiconductor device can be attained.
[0026] (e) Si layer thickness between the aforementioned SiGe distortion impression layer and the SiO2 aforementioned insulating layer turns into thickness below the aforementioned SiGe distortion impression layer, and can attain formation of an effective SiGe distortion impression layer.
[0027] according to the means of the above (2), since in addition to the effect of the aforementioned means (1) SiO2 insulating layer is formed so that the upper surface of the SiO2 aforementioned insulating layer may touch the inferior surface of tongue of the aforementioned distortion impression

layer, reduction of stray capacity can be attained and the property of a field effect transistor improves
[0028] According to the means of the above (3), it can do [manufacturing the semiconductor device which has the modulation dope type field effect transistor which has the aforementioned means (1) or an effect by the composition of (2), or].
[0029] According to the means of the above (4), the new semiconductor substrate excellent in the flat nature of the silicon on insulator (SOI) structure where a front face serves as a mixed-crystal semiconductor layer can be offered. Since this semiconductor substrate serves as the structure of having SiO2 insulating layer which has a mixed-crystal semiconductor layer (SiGe layer) on Si substrate, and was formed in the inner direction of the surface section of Si substrate of pouring of oxygen ion, and annealing processing, In the manufacture, the aforementioned mixed-crystal semiconductor layer thickness can be made thin, and the aforementioned mixed-crystal semiconductor layer is also the difference in a lattice constant with Si (for the lattice constant of Si, the lattice constant of 5.4309A and germanium is 5.6575A). It can consider as the layer which is distorted and acts as an impression layer. Therefore, by use of this semiconductor substrate, micro processing also becomes possible and high integration of a semiconductor device is attained. Moreover, when flat nature is distorted in the aforementioned mixed-crystal semiconductor layer and forms a channel layer from the semiconductor substrate and bird clapper which have the mixed-crystal semiconductor layer which is good, is distorted and turns into an impression layer, manufacture of a high-speed and highly efficient electric field effect type transistor, a modulation dope type field effect transistor, etc. can also be attained by forming a spacer layer, a carrier supply layer, etc. further etc.
[0030] According to the means of the above (5), since a semiconductor substrate has composition whose upper surface of the SiO2 aforementioned insulating layer corresponds with the inferior surface of tongue of the aforementioned mixed-crystal semiconductor layer while having the effect of the semiconductor substrate by the composition of the aforementioned means (4), it can attain reduction of stray capacity.
[0031]
[Embodiments of the Invention] Hereafter, with reference to a drawing, the gestalt of operation of this invention is explained in detail. In addition, in the complete diagram for explaining the gestalt of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.
[0032] (Operation gestalt 1) Drawing 1 or drawing 5 is drawing concerning the semiconductor device which is 1 operation gestalt (operation gestalt 1) of this invention, and drawing 1 is a typical cross section in each process [in / manufacture of a semiconductor device / in the typical cross section, drawing 2 , or drawing 5 of a semiconductor device].
[0033] This operation gestalt 1 explains the semiconductor device which has a field effect transistor. Drawing 1 or drawing 5 is drawing showing only a field-effect-transistor portion.
[0034] The semiconductor device 100 of this operation gestalt 1 has the structure where laminating growth of the SiGe distortion impression layer 102 and the distortion Si channel layer 104 which become the upper front face (principal plane) of the Si substrate 101 from Si1-xGex (0<=x<=1) was carried out one by one, as shown in drawing 1 . Moreover, in the surface section of the Si substrate 101, it has the structure of having SiO2 insulating layer 103 in the interior.
[0035] Moreover, the isolation insulating region 105 to which it penetrates to a part for Si layer on the aforementioned distortion Si channel layer 104, the SiGe distortion impression layer 102, and SiO2 insulating layer 103, and a bottom reaches the SiO2 aforementioned insulating layer 103 is formed. The diffusion field 108 of the couple which constitutes the source field and drain field of a field effect transistor is established in the element formation field 121 surrounded by the aforementioned isolation insulating region 105.
[0036] Moreover, the gate oxide film 106 is formed in the front face of the distortion Si channel layer 104 between the diffusion fields 108 of the aforementioned couple. The gate electrode 107 is formed on this gate oxide film 106, and the side attachment wall (sidewall) 122 which consists of an insulator is formed in the ends of the gate oxide film 106 and the gate electrode 107. The aforementioned diffusion field 108 is established in the ends side of the aforementioned gate oxide film 106, respectively.
[0037] The layer insulation film 109 is formed on the aforementioned distortion Si channel layer 104, the gate electrode 107, and the side attachment wall 122. While the contact hole is prepared in this layer

insulation film 109, the metal wiring 111 is formed in this contact hole portion, the gate wiring connected to the gate electrode 107 and the wiring the source connected to the diffusion field 108 and for drains are formed, and the field effect transistor is constituted.

[0038] Next, the manufacture method of the semiconductor device of this operation gestalt 1, composition of each component, a size, etc. are explained, referring to drawing 2 or drawing 5 .

[0039] First, as shown in drawing 2 , the Si substrate 101 with a thickness of hundreds of micrometers is prepared. Then, the aforementioned Si substrate 101 is washed and it is made the pure Si substrate 101.

[0040] Next, after washing, it introduces into chemical-vapor-deposition equipment (CVD system) immediately, and as shown in drawing 2 , the SiGe distortion impression layer (SiGe buffer layer) 102 which consists of an Si1-xGex mixed-crystal layer (0<=x<=1) is formed on the flat 1 front face (principal plane) of the aforementioned Si substrate 101. With this operation gestalt 1, the aforementioned mixed-crystal ratio x is set to 0.3. Therefore, the SiGe distortion impression layer 102 turns into the Si0.7germanium0.3 distortion impression layer 102. For example, it is made to grow up to be a raw material at the growth temperature of 500 degrees C using SiH4 and GeH4, and is made to grow up to be the thickness of 150nm in CVD.

[0041] The formation method of the Si0.7germanium0.3 distortion impression layer 102 (mixed-crystal ratio x) should just be the method of forming the SiGe layer of not only a chemical-vapor-deposition method but a high grade. When reduction of an isolation performance or stray capacity is taken into consideration, as for the thickness of a SiGe layer, it is desirable to be referred to as about 50 - 200nm. Moreover, although the composition ratio of Si and germanium is fundamentally arbitrary since SiGe alloys are all rate dissolution systems, it is desirable to give the suitable distortion for Si channel layer, and for germanium ratio (mixed-crystal ratio x) to make it to about 40% from 10% as a suitable value to maintain the flat nature of Si channel layer. Moreover, what germanium composition is changed also for toward the direction of thickness (inclination composition) is effective.

[0042] Next, while pouring in oxygen ion from the SiGe distortion impression layer 102 on condition that acceleration voltage 200KeV and 4x1017/cm2 of doses, annealing is performed at 1300 degrees C after that for 8 hours. Thereby, as shown in drawing 3 , SiO2 insulating layer 103 is formed in the surface portion of the Si substrate [directly under] 101 of the SiGe distortion impression layer 102. The thickness of SiO2 insulating layer 103 is about 100nm, and more than isolation voltage 50V is secured. By the aforementioned annealing processing, the SiGe distortion impression layer 102 has very low defect density, and it is flat, and distortion relief is fully made.

[0043] Here, the pouring depth (peak position of an oxygen density profile) of oxygen ion is very important. If the distance of SiO2 insulating layer and Si channel is close brought if possible since it is advantageous to reduction of stray capacity etc., i.e., the pouring depth is made shallow and oxygen will be poured in into a SiGe layer, it not only becomes impossible to maintain sufficient insulation, but alternative oxidization of Si and a deposit of germanium will take place in heat treatment process, and surface flat nature will get worse remarkably. Then, the pouring depth of oxygen ion needs to make it the interior of directly under [of a SiGe layer], and Si. If it carries out like this, in heat treatment process, it will excel in insulation and flat SiO two-layer will be formed. in heat treatment process, the injury by the oxygen ion implantation will recover a SiGe layer, and it is eased, and from before, distortion will be boiled markedly and can form a thin SiGe distortion impression layer Furthermore, it is better for the distance of a SiGe layer and an oxygen ion-implantation position to be so desirable that it be near, for example, to carry out to below the critical thickness (20% of germanium concentration 400nm order and 50% before or after 100nm) of distortion growth of Si and SiGe. By carrying out like this, the SiGe distortion impression layer by which distortion was eased effectively is formed. If this distance is made remarkably thin and the pouring position (peak of a concentration profile) will be contained in Si layer although the skirt of an oxygen ion-implantation concentration profile enters in a SiGe layer, the influence by problems, such as a deposit of germanium which was described above also in the subsequent annealing process, will become very small.

[0044] By this method, it will be more thinly [than before] flat and the very few SiGe distortion impression layer of a crystal defect can form in the upper part of SiO2 insulating layer. In addition, Si layer thickness between the aforementioned SiGe distortion impression layer and the SiO2 aforementioned insulating layer should just be the thickness below the aforementioned SiGe distortion

impression layer.
[0045] Next, as shown in drawing 4 , it is distorted in the upper part of the SiGe distortion impression layer 102 by the chemical-vapor-deposition method, and Si channel layer 104 is formed in it. Thickness could be 20nm. Since it is distorted in the upper part of the above SiGe distortion impression layers 102 and Si channel layer 104 is formed, in the SiGe distortion impression layer 102, it is fully distorted and is eased, and distortion can be given in eye a flat hatchet and the distortion Si channel layer 104 very effectively, and the crystal-defect density of a channel layer also becomes very small. Moreover, in order to prevent the fall of the mobility by reduction of the punch-through current of a field-effect transistor, and transition generating into a channel layer, as for the distortion Si channel layer 104, it is desirable to make it in general the thickness below the ** (3-2x) nm grade of 10. The lattice constant of the SiGe distortion impression layer 102 pulls from a larger (Si is 5.4309A and germanium is 5.6575A) thing than Si, and, as for this distortion Si channel layer 104, receives distortion. Thereby, the carrier (electron and hole) mobility in this becomes large with 3500 (electron) and 5000 (hole) grades rather than 1500 (electron) of the mobility in undistorted Si, and 500 (hole).
[0046] Next, as shown in drawing 4 , the element formation field 121 which forms the circuit element which forms the isolation insulating region 105 by the technique in ordinary use, and contains a field effect transistor and a field effect transistor is formed. The aforementioned isolation insulating region 105 is formed formation of a trench, and by embedding this trench by the oxide film.
[0047] The element formation field 121 is surrounded by the isolation insulating region 105 in the circumference, since SiO2 insulating layer 103 is formed, the lower part can become the high thing of electric insulation, and it can raise the property of elements, such as a field effect transistor incorporated.
[0048] Next, as shown in drawing 4 , while oxidizing thermally the front face of the distortion Si channel layer 104 and forming an oxide film, after forming a polysilicon contest film in piles, the polysilicon contest film and oxide film of a portion except a gate formation field are **********ed, and the gate oxide film 106 and the gate electrode 107 are formed.
[0049] Next, as shown in drawing 5 , after forming an oxide film in the principal plane side of the aforementioned Si substrate 101, by anisotropic etching, the aforementioned oxide film is removed and a side attachment wall (sidewall) 122 is formed in the both-sides side of the aforementioned gate oxide film 106 and the gate electrode 107.
[0050] Next, as shown in drawing 5 , while preparing a resist in the principal plane side of the Si substrate 101 alternatively, the diffusion field 108 which constitutes a source field and a drain field by the self aryne using the aforementioned side attachment wall 122 is formed.
[0051] Next, as shown in drawing 5 , the layer insulation film 109 is formed, a contact hole 110 is broken, when the vacuum evaporationo of the metal membranes, such as aluminum, is carried out and they carry out patterning, the metal wiring 111 is formed in the contact hole 110 aforementioned portion, and a field-effect transistor is completed (refer to drawing 1).
[0052] In the ion implantation in formation of the aforementioned diffusion field 108, if V group elements, such as P, are poured in, this field effect transistor can form n type field, will serve as an n channel type electric field effect type transistor (NMOS), if III group elements, such as Ga, are poured in, can form p type field and will serve as a p-channel type electric field effect type transistor (PMOS). Therefore, CMOSFET can also be manufactured by forming PMOS and NMOS in the same Si substrate 101.
[0053] The Si substrate 101 shown by drawing 3 manufactured in manufacture of the semiconductor device of this operation gestalt 1 can be marketed as a semiconductor substrate in the state with this.
[0054] That is, this semiconductor substrate is the structure of having SiO2 insulating layer 103 in the direction in the surface portion of the Si substrate 101 while having the SiGe distortion impression layer 102 in the principal plane of the Si substrate 101. And the SiGe distortion impression layer 102 of the size of each part is about 50-200nm in thickness as mentioned above, and SiO2 insulating layer 103 is about 100nm. Moreover, Si layer thickness between the SiGe distortion impression layer 102 and the SiO2 aforementioned insulating layer 103 is the thickness below the aforementioned SiGe distortion impression layer.
[0055] According to this operation gestalt 1, the following effects are done so.
(1) Although the structure of a field effect transistor becomes the thing excellent in the same isolation

nature as the field effect transistor manufactured using the SIMOX substrate, thickness of the SiGe distortion impression layer 102 is thinly made with about 200nm or less below the half as compared with about 500nm or more of a SIMOX substrate, and flat nature becomes good. Consequently, the penetration transposition of a SiGe distortion impression layer, generating of a crack, and aggravation of front-face nature can be prevented, and hetero structure with good crystallinity can be realized. Moreover, the distortion Si channel layer 104 formed on the SiGe distortion impression layer 102 can also be made thin below the ** (3-2x) nm grade of 10 from flattening of the SiGe distortion impression layer 102. Therefore, the fall of the mobility by reduction of the punch-through current of a field-effect transistor and transition generating into a channel layer can be prevented, and improvement in the speed of a field effect transistor and highly efficient-ization can be attained.

[0056] (2) With the above (1), flattening of the SiGe distortion impression layer 102 can be attained, thin-shape-izing of the distortion Si channel layer 104 to micro processing becomes possible, and high integration can be attained.

[0057] (3) By thin shape-ization of the SiGe distortion impression layer 102 and the distortion Si channel layer 104, shortening of film formation time can be aimed at and reduction of the manufacturing cost of a semiconductor device can be attained.

[0058] (4) Si layer thickness between the SiGe distortion impression layer 102 and SiO2 insulating layer 103 turns into 102 or less aforementioned SiGe distortion impression layer thickness, and can attain formation of the effective SiGe distortion impression layer 102.

[0059] (5) The new semiconductor substrate excellent in the flat nature of the silicon on insulator (SOI) structure where a front face serves as a SiGe mixed-crystal semiconductor layer can be offered. Since this semiconductor substrate serves as the structure of having SiO2 insulating layer 103 which has the SiGe distortion impression layer 102 on the Si substrate 101, and was formed in the inner direction of the surface section of the Si substrate 101 of pouring of oxygen ion, and annealing processing, It can consider as the layer which thickness of the aforementioned SiGe distortion impression layer 102 can be made thin in the manufacture, and the aforementioned SiGe distortion impression layer 102 is also distorted by the difference in a lattice constant with Si (the lattice constant of 5.4309A and germanium is 5.6575A for the lattice constant of Si), and acts as an impression layer. Therefore, by use of this semiconductor substrate, micro processing of a semiconductor device also becomes possible and high integration of a semiconductor device is attained. Moreover, when flat nature is distorted in the aforementioned mixed-crystal semiconductor layer and forms a channel layer from the semiconductor substrate and bird clapper which have the mixed-crystal semiconductor layer which is good, is distorted and turns into an impression layer, manufacture of a high-speed and highly efficient electric field effect type transistor can be attained. Moreover, manufacture of a high-speed and highly efficient modulation dope type field effect transistor etc. can also be attained by forming a spacer layer, a carrier supply layer, a cap layer, etc. on the aforementioned distortion Si channel layer 104 so that it may mention later etc.

[0060] (Operation gestalt 2) Drawing 6 is the typical cross section showing the semiconductor device which are other operation gestalten (operation gestalt 2) of this invention. With this operation gestalt 2, it sets to the field effect transistor of the aforementioned operation gestalt 1. The ** which does not make Si layer intervene between SiO2 insulating layer 103 and the SiGe distortion impression layer 102, In case oxygen ion is poured in and annealed from the front face of the time 102 of formation of SiO2 insulating layer 103, i.e., the SiGe distortion impression layer on the Si substrate 101, by control of the pouring depth of oxygen ion, and control of annealing processing SiO2 insulating layer 103 is formed so that the upper surface of SiO2 insulating layer 103 may be in agreement with the inferior surface of tongue of the SiGe distortion impression layer 102.

[0061] With such structure, in addition to the effect of the aforementioned operation gestalt 1, reduction of stray capacity can be attained, and improvement in the property of a field effect transistor can be attained.

[0062] Moreover, in manufacture of the semiconductor device of this operation gestalt 2, the thing of the stage in which SiO2 insulating layer 103 was formed can be marketed as a semiconductor substrate. Drawing 7 is the cross section of the semiconductor substrate 130 with the new structure whose upper surface of SiO2 insulating layer 103 corresponded with the inferior surface of tongue of the SiGe distortion impression layer 102. The semiconductor substrate 130 of this structure can also be

marketed as it is, this semiconductor substrate 130 can be used, and the semiconductor device which has a field effect transistor, the modulation dope type field effect transistor mentioned later can be manufactured.

[0063] (Operation gestalt 3) This operation gestalt 3 explains the semiconductor device which has a modulation dope type field effect transistor. The typical cross section, drawing 9 , or drawing 12 which shows the field effect transistor of a modulation dope type [drawing 8] is the typical cross section showing the manufacture method of the modulation dope type field effect transistor of this operation gestalt 3.

[0064] The semiconductor device 140 of this operation gestalt 3 is set to the semiconductor device 100 of the aforementioned operation gestalt 1. On the distortion Si channel layer 104 The Si1-xGex mixed crystal of 15nm of thickness The SiGe spacer layer 211 which consists of (0<=x<=1), the SiGe carrier supply layer (carrier doping layer) 212 which consists of Si1-xGex mixed crystal (0<=x<=1) which doped Sb of 5nm of thickness, the Si1-xGex mixed crystal of 10nm of thickness It has the structure of having the SiGe cap layer 213 which consists of (0<=x<=1), and Si cap layer 214 which consists of Si of 5nm of thickness. The aforementioned mixed-crystal ratio x is 0.3.

[0065] Moreover, on Si cap layer 214 of the element formation field 121 surrounded by the isolation insulating region 105, the gate oxide film 106 which has a side attachment wall 122, and the gate electrode 107 are formed in ends. The diffusion field 108 which turns into a source field or a drain field is established in the ends side of the gate oxide film 106. This diffusion field 108 has structure which reaches by Fukashi in the middle of the distortion Si channel layer 104.

[0066] As manufacture of the semiconductor device 140 of this operation gestalt 3 is shown in drawing 9 , it is the Si substrate 101. The semiconductor substrate which has the SiGe distortion impression layer 102 in a principal plane, and has SiO2 insulating layer 103 in the direction in the surface portion of the Si substrate 101 is manufactured. This manufacture method is the same as that of the aforementioned operation gestalt 1, and is the completely same structure as drawing 3 .

[0067] As shown in drawing 10 , on the aforementioned distortion Si channel layer 104 next, by the chemical-vapor-deposition method The Si1-xGex mixed crystal of 15nm of thickness The SiGe spacer layer 211 which consists of (x= 0.3), the SiGe carrier supply layer (carrier doping layer) 212 which consists of Si1-xGex mixed crystal (x= 0.3) which doped Sb of 5nm of thickness, the Si1-xGex mixed crystal of 10nm of thickness Growth formation of the SiGe cap layer 213 which consists of (x= 0.3), and the Si cap layer 214 which consists of Si of 5nm of thickness is carried out one by one.

[0068] Next, as shown in drawing 11 , the isolation insulating region 105 is formed by the technique in ordinary use, and it is the element formation field 121. It forms. The aforementioned isolation insulating region 105 is formed formation of a trench, and by embedding this trench by the oxide film.

[0069] Next, as shown in drawing 11 , while oxidizing thermally the front face of the aforementioned Si cap layer 214 and forming an oxide film, after forming a polysilicon contest film in piles, as it **********s and the polysilicon contest film and oxide film of a portion except a gate formation field are shown in drawing 12 , the gate oxide film 106 and the gate electrode 107 are formed.

[0070] Next, illustration is the aforementioned gate oxide film 106 like the case where it is the aforementioned operation gestalt 1 although not carried out. And after forming a side attachment wall (sidewall) 122 in the both-sides side of the gate electrode 107, The diffusion field 108 which constitutes a source field and a drain field from a method in ordinary use by the self aryne using a side attachment wall 122 is formed. Subsequently, the layer insulation film 109 is formed, a contact hole is broken, the metal wiring 111 is formed in the aforementioned contact hole portion by carrying out the vacuum evaporationo of the metal membranes, such as aluminum, and carrying out patterning, and an n type modulation dope type field effect transistor as shown in drawing 8 is formed. The aforementioned diffusion field 108 is formed so that it may reach by Fukashi in the middle of the distortion Si channel layer 104.

[0071] Moreover, in the ion implantation in formation of the aforementioned diffusion field 108, if an III group element is poured in, a p-channel type modulation dope type field effect transistor can be manufactured.

[0072] Also in the modulation dope type field effect transistor by this operation gestalt 3, flattening becomes good by thin shape-ization of the SiGe distortion impression layer 102, the distortion Si channel layer 104 formed on the SiGe distortion impression layer 102 can also be made thin below the

** (3-2x) nm grade of 10, the fall of the mobility by reduction of punch-through current and transition generating into a channel layer can be prevented, and improvement in the speed of a field effect transistor and highly efficient-ization can be attained.
[0073] Moreover, thin-shape-izing of the distortion Si channel layer 104 by flattening of the SiGe distortion impression layer 102 to micro processing becomes possible, and high integration can be attained.
[0074] Moreover, by thin shape-ization of the SiGe distortion impression layer 102 and the distortion Si channel layer 104, shortening of film formation time can be aimed at and it will have the effect of being able to attain reduction of the manufacturing cost of a semiconductor device.
[0075] also in this operation gestalt 3, reduction of the stray capacity of the field effect transistor of especially more a modulation dope type which adopts the technology which forms SiO2 insulating layer 103 so that the upper surface of SiO2 insulating layer 103 may be in agreement with the inferior surface of tongue of the SiGe distortion impression layer 102 can be attained
[0076] Although invention made by this invention person above explained concretely based on an operation gestalt, this invention is not limited to the above-mentioned operation gestalt, and the same effect as the aforementioned example is acquired also by the case of the semiconductor device which it could not be overemphasized that it can change variously in the range which does not deviate from the summary, for example, formed other mixed-crystal semiconductor layers, such as GaAs, as a distortion impression layer 102 which forms on an Si substrate 101.
[0077] Although the above explanation explained the case where invention mainly made by this invention person was applied to the manufacturing technology of the field effect transistor which is a field of the invention used as the background, it is not limited to it.
[0078] this invention is applicable to manufacture of the semiconductor device which has active elements, such as a transistor and diode, at least.
[0079]
[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
(1) Compared with the former, the semiconductor device which contains the field-effect transistor and this by this invention has low punch-through current, and can decrease [that the defect density of a channel portion decreases remarkably, and] the thickness of a distortion impression layer (buffer layer) conventionally, and is excellent in the flat nature of a channel portion. That is, since improvement in the speed of an element, high integration, and highly efficient-ization can be attained, the industrial value is very high.

[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] Especially this invention is applied to the manufacturing technology of the semiconductor device containing a SiGe hetero structure transistor about the manufacture method of the manufacture method of a semiconductor device and a semiconductor device, a semiconductor substrate, and a semiconductor substrate, and relates to effective technology.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In connection with the densification of an integrated circuit, the size reduction and the improvement in speed in Si field-effect transistor serve as pressing need. On the other hand, development of the high-speed low-power transistor for communication is also desired

strongly.
[0003] it is distorted and the thing which was made to impress distortion to Si channel and which boil Si (hetero structure) transistor markedly compared with the conventional Si field-effect transistor, and can accelerate is suggested (M. V.Fischetti and S.E.Laux:J.Appl.Phys.80 (1996) 2234)
[0004] In the hetero structure transistor formed on Si substrate, in order to give distortion to a channel layer, it is necessary to prepare the buffer layer (distortion impression layer) from which this and a lattice constant differ in the lower part of a channel layer. Although Si1-xGex mixed crystal (0<=x<=1) was conventionally used as a buffer layer, realization of the high mobility transistor which needs to carry out the laminating of the buffer layer with a thickness of 1 microns or more, has a bad influence on the transport properties of a channel layer for aggravation of the problem which dislocation penetrates to the buffer-layer upper part, or surface roughness, and has desired electronic transport properties was difficult.
[0005] Moreover, it is related with the transistor (field effect transistor) using Si and germanium. EKUSUTENDEDO Abstract OBU 1993 International Conference ON Solid state Device and -- MATERIARUZU, MAKUHARI, 1993, and the 201st A page to the 203rd It is discussed by the page (Extended Abstravts of the 1993 International Conference on Solid State Devices and Materials, Makuhari(1993) pp.201-203).
[0006] The field effect transistor (high mobility transistor) indicated by this reference has the structure of having a SiGe buffer layer on Si substrate, and having Si channel layer and a SiGe layer on this SiGe buffer layer. Moreover, the delta dope layer (electronic supply layer) which consists of a single atomic layer which doped Sb is prepared in the middle of the aforementioned SiGe layer.
[0007] SOI which considered high-speed operation and prepared the silicon layer on the electric insulating plate on the other hand Using a substrate is examined. SOI SIMOX which anneals after injecting oxygen ion into Si substrate, although some methods, such as a lamination substrate, are proposed by the substrate, and forms an oxide layer Promising ** of the method is carried out. SIMOX Using a substrate is distorted only not only in the conventional Si field-effect transistor, and it brings about a big advantage also in production of Si transistor.
[0008] That is, if a SiGe distortion impression layer is formed on a SIMOX substrate, since many dislocation occurs in Si layer of the SiO2 and the upper part of those in a substrate, it will become possible to make the dislocation density of a SiGe layer mitigate. However, for reduction of dislocation density, also at the lowest, the thickness of a SiGe layer is 500nm or more need, and is not desirable because of the flat nature on the front face of a film, or productivity.
[0009] Thus, formation of a quality distorted impression layer required for realization of a high-speed SiGe hetero structure quantity mobility transistor (HEMT) with the conventional technology was difficult. In addition, the example which formed the field effect transistor and the high mobility transistor using the SIMOX substrate is indicated by D.KNayak, J.S.Park, J.C.S.Woo, KL.Wang, G.KYabiku, and and KP.MacWilliams International Electron Devices Meeting (IEDM).

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
(1) Compared with the former, the semiconductor device which contains the field-effect transistor and this by this invention has low punch-through current, and can decrease [that the defect density of a channel portion decreases remarkably, and] the thickness of a distortion impression layer (buffer layer) conventionally, and is excellent in the flat nature of a channel portion. That is, since improvement in the speed of an element, high integration, and highly efficient-ization can be attained, the industrial value is very high.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] With the above-mentioned conventional technology, there are problems, such as penetration dislocation of a buffer layer, aggravation of front-face nature, or productivity aggravation of a buffer layer, and this obstructed realization of a high-speed SiGe hetero structure quantity mobility transistor.
[0011] The purpose of this invention is by realizing hetero structure with good crystallinity to offer the manufacture method of a semiconductor device excellent in the semiconductor device and productivity which have the hetero structure transistor which can attain improvement in the speed, highly-efficient-izing, and high integration.
[0012] Other purposes of this invention are to offer Si substrate (semiconductor substrate) of hetero structure with good crystallinity. The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.

[Translation done.]

MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
(1) SiO2 insulating layer which is formed in Si substrate and formed inside the principal plane of the aforementioned Si substrate, It consists of a mixed-crystal semiconductor layer prepared on the principal plane of the aforementioned Si substrate, and is distorted. An impression layer, The diffusion field of the couple which is distorted, is prepared in a channel layer and the aforementioned distortion channel layer, and constitutes a source field or a drain field which consists of an Si layer prepared on the aforementioned distortion impression layer, It is the semiconductor device which has the field effect transistor constituted by the gate electrode prepared through a gate insulator layer on the distortion channel layer between the diffusion fields of the aforementioned couple. The aforementioned distortion impression layer consists of Si1-xGex (0<=x<=1), and the aforementioned distortion impression layer becomes the thickness of about 50-200nm. Si layer thickness between the aforementioned Si1-xGex distortion impression layer and the SiO2 aforementioned insulating layer turns into thickness below the aforementioned Si1-xGex distortion impression layer. The aforementioned distortion channel layer thickness has become below the ** (3-2x) nm grade of 10 that is the critical thickness by which Si distorts and grows on Si1-xGex.
[0014] Such an electric field effect type transistor is manufactured by the following manufacture methods. It is formed in Si substrate. Consist of an Si layer between the source fields and drain fields which were established in the aforementioned Si substrate, and it is distorted to it, and have a channel layer, and a gate insulator layer is minded on the distortion channel layer between the aforementioned source field and a drain field. The process which is the manufacture method of a semiconductor device of having the field effect transistor constituted by preparing a gate electrode, and becomes the principal plane of the aforementioned Si substrate from a mixed-crystal semiconductor layer and which is distorted and forms an impression layer, The process which anneals while pouring in oxygen ion from the front face of the aforementioned distortion impression layer, and forms SiO2 insulating layer in the aforementioned Si substrate, It has the process which forms the aforementioned distortion channel layer on the aforementioned distortion impression layer, the process which forms an isolation insulating region and forms an element formation field in the principal plane side of the aforementioned Si substrate, and the process which forms the diffusion field which constitutes the aforementioned gate electrode and a source field, and a drain field in the aforementioned element formation field. Pouring of

the aforementioned oxygen ion and the processing conditions of annealing are chosen, and it forms so that the surface portion of the aforementioned Si substrate may remain between the aforementioned distortion impression layer and the SiO2 aforementioned insulating layer. The aforementioned distortion impression layer is formed in the thickness of 50 - 200 nm, and the aforementioned distortion channel layer thickness is formed below in the ** (3-2x) nm grade of 10.

[0015] (2) In the composition of the aforementioned means (1), it has the structure where the upper surface of the SiO2 aforementioned insulating layer touches the inferior surface of tongue of the aforementioned distortion impression layer. It is formed in Si substrate, and it consists of a mixed-crystal semiconductor layer [an Si1-xGex layer (0<=x<=1)] of the thickness 50 prepared on the principal plane of the aforementioned Si substrate - 200 nm, and is distorted. Namely, an impression layer, SiO2 insulating layer prepared in the aforementioned Si substrate so that the upper surface may extend along with the aforementioned distortion impression layer in contact with the inferior surface of tongue of the aforementioned distortion impression layer, The thickness prepared on the aforementioned distortion impression layer consists of an Si layer below the ** (3-2x) nm grade of 10, and it is distorted. A channel layer, It has the composition of having the field effect transistor constituted by the gate electrode prepared through a gate insulator layer on the distortion channel layer between the diffusion field of the couple which is prepared in the aforementioned distortion channel layer and constitutes a source field or a drain field, and the diffusion field of the aforementioned couple.

[0016] In the manufacture method by the means of the above (1), such an electric field effect type transistor chooses pouring of the aforementioned oxygen ion, and the processing conditions of annealing, and it forms them so that the upper surface of the SiO2 aforementioned insulating layer may be in agreement with the undersurface of the aforementioned distortion impression layer.

[0017] (3) In the aforementioned means (1) or the composition of (2), on the aforementioned distortion channel layer, a spacer layer, the carrier supply layer by which the conductivity-type determination impurity was doped, and a cap layer are formed one by one, and constitute the modulation dope type field effect transistor.

[0018] In the above (1) or the manufacture method by the means of (2), on the aforementioned distortion channel layer, such a modulation dope type field effect transistor forms a spacer layer, the delta carrier supply layer by which the conductivity-type determination impurity was doped, and a cap layer one by one, and forms a modulation dope type field effect transistor.

[0019] (4) The semiconductor substrate which consists of SiO2 insulating layer formed in the principal plane of Si substrate and the aforementioned Si substrate of annealing processing of the oxygen ion poured in from the front face of the mixed-crystal semiconductor layer by which growth formation was carried out, and the aforementioned mixed-crystal semiconductor layer. Between the SiO2 aforementioned insulating layer and the aforementioned mixed-crystal semiconductor layer, Si layer which constitutes Si substrate below the aforementioned mixed-crystal semiconductor layer thickness exists. The aforementioned mixed-crystal semiconductor layer consists of an Si1-xGex layer (0<=x<=1), and the thickness has become 50 - 200 nm.

[0020] Such a semiconductor substrate is manufactured according to the process which pours in oxygen ion so that the peak of a pouring distribution in the aforementioned Si substrate may be located in the principal plane of Si substrate from the process which carries out growth formation of the mixed-crystal semiconductor layer, and the front face of the aforementioned mixed-crystal semiconductor layer, and the process which anneals the aforementioned Si substrate and forms the SiO2 aforementioned insulating layer.

[0021] (5) In the composition of the aforementioned means (1), it has composition whose upper surface of the SiO2 aforementioned insulating layer corresponds with the inferior surface of tongue of the aforementioned mixed-crystal semiconductor layer.

[0022] Although the structure of the (a) field effect transistor becomes the same thing as the field effect transistor manufactured using the SIMOX substrate according to the means of the above (1) As compared with about 500nm or more of a SIMOX substrate, SiGe distortion impression layer thickness is thinly made with about 200nm or less below the half, and, as a result, can form the thin distortion Si channel layer below the ** (3-2x) nm grade of thickness 10 on a SiGe distortion impression layer.

[0023] (b) Since flattening of a SiGe distortion impression layer can be attained and distortion Si channel layer thickness can be made thin below the ** (3-2x) nm grade of 10 with the above (a), the fall

of the mobility by reduction of the punch-through current of a field-effect transistor and transition generating into a channel layer can be prevented, and the improvement in a property (improvement in the speed, highly-efficient-izing) of a field effect transistor can be attained.
[0024] (c) With the above (b), flattening of a SiGe distortion impression layer can be attained, thin-shape-izing of a distortion Si channel layer to micro processing becomes possible, and high integration can be attained.
[0025] (d) With the above (a), shortening of the formation time of a SiGe distortion impression layer and a distortion Si channel layer can be aimed at, and reduction of the manufacturing cost of a semiconductor device can be attained.
[0026] (e) Si layer thickness between the aforementioned SiGe distortion impression layer and the SiO2 aforementioned insulating layer turns into thickness below the aforementioned SiGe distortion impression layer, and can attain formation of an effective SiGe distortion impression layer.
[0027] according to the means of the above (2), since in addition to the effect of the aforementioned means (1) SiO2 insulating layer is formed so that the upper surface of the SiO2 aforementioned insulating layer may touch the undersurface of the aforementioned distortion impression layer, reduction of stray capacity can be attained and the property of a field effect transistor improves
[0028] According to the means of the above (3), it can do [manufacturing the semiconductor device which has the modulation dope type field effect transistor which has the aforementioned means (1) or an effect by the composition of (2), or].
[0029] According to the means of the above (4), the new semiconductor substrate excellent in the flat nature of the silicon on insulator (SOI) structure where a front face serves as a mixed-crystal semiconductor layer can be offered. Since this semiconductor substrate serves as the structure of having SiO2 insulating layer which has a mixed-crystal semiconductor layer (SiGe layer) on Si substrate, and was formed in the inner direction of the surface section of Si substrate of pouring of oxygen ion, and annealing processing, In the manufacture, the aforementioned mixed-crystal semiconductor layer thickness can be made thin, and the aforementioned mixed-crystal semiconductor layer is also the difference in a lattice constant with Si (for the lattice constant of Si, the lattice constant of 5.4309A and germanium is 5.6575A). It can consider as the layer which is distorted and acts as an impression layer. Therefore, by use of this semiconductor substrate, micro processing also becomes possible and high integration of a semiconductor device is attained. Moreover, flat nature is good, and when it is distorted in the aforementioned mixed-crystal semiconductor layer and a channel layer is formed from the semiconductor substrate and bird clapper which have a mixed-crystal semiconductor layer used as a distortion impression layer, manufacture of a high-speed and highly efficient electric field effect type transistor, a modulation dope type field effect transistor, etc. can also be attained by forming a spacer layer, a carrier supply layer, etc. further etc.
[0030] According to the means of the above (5), since a semiconductor substrate has composition whose upper surface of the SiO2 aforementioned insulating layer corresponds with the undersurface of the aforementioned mixed-crystal semiconductor layer while having the effect of the semiconductor substrate by the composition of the aforementioned means (4), it can attain reduction of stray capacity.
[0031]
[Embodiments of the Invention] Hereafter, with reference to a drawing, the form of operation of this invention is explained in detail. In addition, in the complete diagram for explaining the form of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.
[0032] (Operation form 1) Drawing 1 or drawing 5 is drawing concerning the semiconductor device which is 1 operation form (operation form 1) of this invention, and drawing 1 is a typical cross section in each process [in / manufacture of a semiconductor device / in the typical cross section, drawing 2 , or drawing 5 of a semiconductor device].
[0033] This operation form 1 explains the semiconductor device which has a field effect transistor. Drawing 1 or drawing 5 is drawing showing only a field-effect-transistor portion.
[0034] The semiconductor device 100 of this operation form 1 has the structure where laminating growth of the SiGe distortion impression layer 102 and the distortion Si channel layer 104 which become the upper front face (principal plane) of the Si substrate 101 from Si1-xGex (0<=x<=1) was carried out one by one, as shown in drawing 1 . Moreover, in the surface section of the Si substrate

101, it has the structure of having SiO2 insulating layer 103 in the interior.
[0035] Moreover, the isolation insulating region 105 to which it penetrates to a part for Si layer on the aforementioned distortion Si channel layer 104, the SiGe distortion impression layer 102, and SiO2 insulating layer 103, and a bottom reaches the SiO2 aforementioned insulating layer 103 is formed. The diffusion field 108 of the couple which constitutes the source field and drain field of a field effect transistor is established in the element formation field 121 surrounded by the aforementioned isolation insulating region 105.
[0036] Moreover, the gate oxide film 106 is formed in the front face of the distortion Si channel layer 104 between the diffusion fields 108 of the aforementioned couple. The gate electrode 107 is formed on this gate oxide film 106, and the side attachment wall (sidewall) 122 which consists of an insulator is formed in the ends of the gate oxide film 106 and the gate electrode 107. The aforementioned diffusion field 108 is established in the ends side of the aforementioned gate oxide film 106, respectively.
[0037] The layer insulation film 109 is formed on the aforementioned distortion Si channel layer 104, the gate electrode 107, and the side attachment wall 122. While the contact hole is prepared in this layer insulation film 109, the metal wiring 111 is formed in this contact hole portion, the gate wiring connected to the gate electrode 107 and the wiring the source connected to the diffusion field 108 and for drains are formed, and the field effect transistor is constituted.
[0038] Next, the manufacture method of the semiconductor device of this operation form 1, composition of each component, a size, etc. are explained, referring to drawing 2 or drawing 5 .
[0039] First, as shown in drawing 2 , the Si substrate 101 with a thickness of hundreds of micrometers is prepared. Then, the aforementioned Si substrate 101 is washed and it is made the pure Si substrate 101.
[0040] Next, after washing, it introduces into chemical-vapor-deposition equipment (CVD system) immediately, and as shown in drawing 2 , the SiGe distortion impression layer (SiGe buffer layer) 102 which consists of an Si1-xGex mixed-crystal layer (0<=x<=1) is formed on the flat 1 front face (principal plane) of the aforementioned Si substrate 101. With this operation form 1, the aforementioned mixed-crystal ratio x is set to 0.3. Therefore, the SiGe distortion impression layer 102 turns into the Si0.7germanium0.3 distortion impression layer 102. For example, it is made to grow up to be a raw material at the growth temperature of 500 degrees C using SiH4 and GeH4, and is made to grow up to be the thickness of 150nm in CVD.
[0041] The formation method of the Si0.7germanium0.3 distortion impression layer 102 (mixed-crystal ratio x) should just be the method of forming the SiGe layer of not only a chemical-vapor-deposition method but a high grade. When reduction of an isolation performance or stray capacity is taken into consideration, as for the thickness of a SiGe layer, it is desirable to be referred to as about 50 - 200nm. Moreover, although the composition ratio of Si and germanium is fundamentally arbitrary since SiGe alloys are all rate dissolution systems, it is desirable to give the suitable distortion for Si channel layer, and for germanium ratio (mixed-crystal ratio x) to make it to about 40% from 10% as a suitable value to maintain the flat nature of Si channel layer. Moreover, what germanium composition is changed also for toward the direction of thickness (inclination composition) is effective.
[0042] Next, while pouring in oxygen ion from the SiGe distortion impression layer 102 on condition that acceleration voltage 200KeV and 4x1017/cm2 of doses, annealing is performed at 1300 degrees C after that for 8 hours. Thereby, as shown in drawing 3 , SiO2 insulating layer 103 is formed in the surface portion of the Si substrate [directly under] 101 of the SiGe distortion impression layer 102. The thickness of SiO2 insulating layer 103 is about 100nm, and more than isolation voltage 50V is secured. By the aforementioned annealing processing, the SiGe distortion impression layer 102 has very low defect density, and it is flat, and distortion relief is fully made.
[0043] Here, the pouring depth (peak position of an oxygen density profile) of oxygen ion is very important. If the distance of SiO2 insulating layer and Si channel is close brought if possible since it is advantageous to reduction of stray capacity etc., i.e., the pouring depth is made shallow and oxygen will be poured in into a SiGe layer, it not only becomes impossible to maintain sufficient insulation, but alternative oxidization of Si and a deposit of germanium will take place in heat treatment process, and surface flat nature will get worse remarkably. Then, the pouring depth of oxygen ion needs to make it the interior of directly under [of a SiGe layer], and Si. If it carries out like this, in heat treatment process, it will excel in insulation and flat SiO two-layer will be formed. in heat treatment process,

damage by the oxygen ion implantation will recover a SiGe layer, and it is eased, and from before, distortion will be boiled markedly and can form a thin SiGe distortion impression layer Furthermore, it is better for the distance of a SiGe layer and an oxygen ion-implantation position to be so desirable that it be near, for example, to carry out to below the critical thickness (20% of germanium concentration 400nm order and 50% before or after 100nm) of distortion growth of Si and SiGe. By carrying out like this, the SiGe distortion impression layer by which distortion was eased effectively is formed. If this distance is made remarkably thin and the pouring position (peak of a concentration profile) will be contained in Si layer although the skirt of an oxygen ion-implantation concentration profile enters in a SiGe layer, the influence by problems, such as a deposit of germanium which was described above also in the subsequent annealing process, will become very small.

[0044] By this method, it will be more thinly [than before] flat and the very few SiGe distortion impression layer of a crystal defect can form in the upper part of SiO2 insulating layer. In addition, Si layer thickness between the aforementioned SiGe distortion impression layer and the SiO2 aforementioned insulating layer should just be the thickness below the aforementioned SiGe distortion impression layer.

[0045] Next, as shown in drawing 4 , it is distorted in the upper part of the SiGe distortion impression layer 102 by the chemical-vapor-deposition method, and Si channel layer 104 is formed in it. Thickness could be 20nm. Since it is distorted in the upper part of the above SiGe distortion impression layers 102 and Si channel layer 104 is formed, in the SiGe distortion impression layer 102, it is fully distorted and is eased, and distortion can be given in eye a flat hatchet and the distortion Si channel layer 104 very effectively, and the crystal-defect density of a channel layer also becomes very small. Moreover, in order to prevent the fall of the mobility by reduction of the punch-through current of a field-effect transistor, and transition generating into a channel layer, as for the distortion Si channel layer 104, it is desirable to make it in general the thickness below the ** (3-2x) nm grade of 10. The lattice constant of the SiGe distortion impression layer 102 pulls from a larger (Si is 5.4309A and germanium is 5.6575A) thing than Si, and, as for this distortion Si channel layer 104, receives distortion. Thereby, the carrier (electron and hole) mobility in this becomes large with 3500 (electron) and 5000 (hole) grades rather than 1500 (electron) of the mobility in undistorted Si, and 500 (hole).

[0046] Next, as shown in drawing 4 , the element formation field 121 which forms the circuit element which forms the isolation insulating region 105 by the technique in ordinary use, and contains a field effect transistor and a field effect transistor is formed. The aforementioned isolation insulating region 105 is formed formation of a trench, and by embedding this trench by the oxide film.

[0047] The element formation field 121 is surrounded by the isolation insulating region 105 in the circumference, since SiO2 insulating layer 103 is formed, the lower part can become the high thing of electric insulation, and it can raise the property of elements, such as a field effect transistor incorporated.

[0048] Next, as shown in drawing 4 , while oxidizing thermally the front face of the distortion Si channel layer 104 and forming an oxide film, after forming a polysilicon contest film in piles, the polysilicon contest film and oxide film of a portion except a gate formation field are **********ed, and the gate oxide film 106 and the gate electrode 107 are formed.

[0049] Next, as shown in drawing 5 , after forming an oxide film in the principal plane side of the aforementioned Si substrate 101, by anisotropic etching, the aforementioned oxide film is removed and a side attachment wall (sidewall) 122 is formed in the both-sides side of the aforementioned gate oxide film 106 and the gate electrode 107.

[0050] Next, as shown in drawing 5 , while preparing a resist in the principal plane side of the Si substrate 101 alternatively, the diffusion field 108 which constitutes a source field and a drain field by the self aryne using the aforementioned side attachment wall 122 is formed.

[0051] Next, as shown in drawing 5 , the layer insulation film 109 is formed, a contact hole 110 is broken, when the vacuum evaporationo of the metal membranes, such as aluminum, is carried out and they carry out patterning, the metal wiring 111 is formed in the contact hole 110 aforementioned portion, and a field-effect transistor is completed (refer to drawing 1).

[0052] In the ion implantation in formation of the aforementioned diffusion field 108, if V group elements, such as P, are poured in, this field effect transistor can form n type field, will serve as an n channel type electric field effect type transistor (NMOS), if III group elements, such as Ga, are poured

in, can form p type field and will serve as a p-channel type electric field effect type transistor (PMOS). Therefore, CMOSFET can also be manufactured by forming PMOS and NMOS in the same Si substrate 101.

[0053] The Si substrate 101 shown by drawing 3 manufactured in manufacture of the semiconductor device of this operation form 1 can be marketed as a semiconductor substrate in the state with this.

[0054] That is, this semiconductor substrate is the structure of having SiO2 insulating layer 103 in the direction in the surface portion of the Si substrate 101 while having the SiGe distortion impression layer 102 in the principal plane of the Si substrate 101. And the SiGe distortion impression layer 102 of the size of each part is about 50-200nm in thickness as mentioned above, and SiO2 insulating layer 103 is about 100nm. Moreover, Si layer thickness between the SiGe distortion impression layer 102 and the SiO2 aforementioned insulating layer 103 is the thickness below the aforementioned SiGe distortion impression layer.

[0055] According to this operation form 1, the following effects are done so.

(1) Although the structure of a field effect transistor becomes the thing excellent in the same isolation nature as the field effect transistor manufactured using the SIMOX substrate, thickness of the SiGe distortion impression layer 102 is thinly made with about 200nm or less below the half as compared with about 500nm or more of a SIMOX substrate, and flat nature becomes good. Consequently, the penetration dislocation of a SiGe distortion impression layer, generating of a crack, and aggravation of front-face nature can be prevented, and hetero structure with good crystallinity can be realized. Moreover, the distortion Si channel layer 104 formed on the SiGe distortion impression layer 102 can also be made thin below the ** (3-2x) nm grade of 10 from flattening of the SiGe distortion impression layer 102. Therefore, the fall of the mobility by reduction of the punch-through current of a field-effect transistor and transition generating into a channel layer can be prevented, and improvement in the speed of a field effect transistor and highly efficient-ization can be attained.

[0056] (2) With the above (1), flattening of the SiGe distortion impression layer 102 can be attained, thin-shape-izing of the distortion Si channel layer 104 to micro processing becomes possible, and high integration can be attained.

[0057] (3) By thin shape-ization of the SiGe distortion impression layer 102 and the distortion Si channel layer 104, shortening of film formation time can be aimed at and reduction of the manufacturing cost of a semiconductor device can be attained.

[0058] (4) Si layer thickness between the SiGe distortion impression layer 102 and SiO2 insulating layer 103 turns into 102 or less aforementioned SiGe distortion impression layer thickness, and can attain formation of the effective SiGe distortion impression layer 102.

[0059] (5) The new semiconductor substrate excellent in the flat nature of the silicon on insulator (SOI) structure where a front face serves as a SiGe mixed-crystal semiconductor layer can be offered. Since this semiconductor substrate serves as the structure of having SiO2 insulating layer 103 which has the SiGe distortion impression layer 102 on the Si substrate 101, and was formed in the inner direction of the surface section of the Si substrate 101 of pouring of oxygen ion, and annealing processing, It can consider as the layer which thickness of the aforementioned SiGe distortion impression layer 102 can be made thin in the manufacture, and the aforementioned SiGe distortion impression layer 102 is also distorted by the difference in a lattice constant with Si (the lattice constant of 5.4309A and germanium is 5.6575A for the lattice constant of Si), and acts as an impression layer. Therefore, by use of this semiconductor substrate, micro processing of a semiconductor device also becomes possible and high integration of a semiconductor device is attained. Moreover, flat nature is good, and when it is distorted in the aforementioned mixed-crystal semiconductor layer and a channel layer is formed from the semiconductor substrate and bird clapper which have a mixed-crystal semiconductor layer used as a distortion impression layer, manufacture of a high-speed and highly efficient electric field effect type transistor can be attained. Moreover, manufacture of a high-speed and highly efficient modulation dope type field effect transistor etc. can also be attained by forming a spacer layer, a carrier supply layer, a cap layer, etc. on the aforementioned distortion Si channel layer 104 so that it may mention later etc.

[0060] (Operation form 2) Drawing 6 is the typical cross section showing the semiconductor device which are other operation forms (operation form 2) of this invention. With this operation form 2, it sets to the field effect transistor of the aforementioned operation form 1. The ** which does not make Si layer intervene between SiO2 insulating layer 103 and the SiGe distortion impression layer 102, In case

oxygen ion is poured in and annealed from the front face of the time 102 of formation of SiO2 insulating layer 103, i.e., the SiGe distortion impression layer on the Si substrate 101, by control of the pouring depth of oxygen ion, and control of annealing processing SiO2 insulating layer 103 is formed so that the upper surface of SiO2 insulating layer 103 may be in agreement with the undersurface of the SiGe distortion impression layer 102.

[0061] With such structure, in addition to the effect of the aforementioned operation form 1, reduction of stray capacity can be attained, and improvement in the property of a field effect transistor can be attained.

[0062] Moreover, in manufacture of the semiconductor device of this operation form 2, the thing of the stage in which SiO2 insulating layer 103 was formed can be marketed as a semiconductor substrate. Drawing 7 is the cross section of the semiconductor substrate 130 with the new structure whose upper surface of SiO2 insulating layer 103 corresponded with the undersurface of the SiGe distortion impression layer 102. The semiconductor substrate 130 of this structure can also be marketed as it is, this semiconductor substrate 130 can be used, and the semiconductor device which has a field effect transistor, the modulation dope type field effect transistor mentioned later can be manufactured.

[0063] (Operation form 3) This operation form 3 explains the semiconductor device which has a modulation dope type field effect transistor. The typical cross section, drawing 9 , or drawing 12 which shows the field effect transistor of a modulation dope type [drawing 8] is the typical cross section showing the manufacture method of the modulation dope type field effect transistor of this operation form 3.

[0064] The semiconductor device 140 of this operation form 3 is set to the semiconductor device 100 of the aforementioned operation form 1. On the distortion Si channel layer 104 The Si1-xGex mixed crystal of 15nm of thickness The SiGe spacer layer 211 which consists of (0<=x<=1), the SiGe carrier supply layer (carrier doping layer) 212 which consists of Si1-xGex mixed crystal (0<=x<=1) which doped Sb of 5nm of thickness, the Si1-xGex mixed crystal of 10nm of thickness It has the structure of having the SiGe cap layer 213 which consists of (0<=x<=1), and Si cap layer 214 which consists of Si of 5nm of thickness. The aforementioned mixed-crystal ratio x is 0.3.

[0065] Moreover, on Si cap layer 214 of the element formation field 121 surrounded by the isolation insulating region 105, the gate oxide film 106 which has a side attachment wall 122, and the gate electrode 107 are formed in ends. The diffusion field 108 which turns into a source field or a drain field is established in the ends side of the gate oxide film 106. This diffusion field 108 has structure which reaches by Fukashi in the middle of the distortion Si channel layer 104.

[0066] As manufacture of the semiconductor device 140 of this operation form 3 is shown in drawing 9 , it is the Si substrate 101. The semiconductor substrate which has the SiGe distortion impression layer 102 in a principal plane, and has SiO2 insulating layer 103 in the direction in the surface portion of the Si substrate 101 is manufactured. This manufacture method is the same as that of the aforementioned operation form 1, and is the completely same structure as drawing 3 .

[0067] As shown in drawing 10 , on the aforementioned distortion Si channel layer 104 next, by the chemical-vapor-deposition method The Si1-xGex mixed crystal of 15nm of thickness The SiGe spacer layer 211 which consists of (x= 0.3), the SiGe carrier supply layer (carrier doping layer) 212 which consists of Si1-xGex mixed crystal (x= 0.3) which doped Sb of 5nm of thickness, the Si1-xGex mixed crystal of 10nm of thickness Growth formation of the SiGe cap layer 213 which consists of (x= 0.3), and the Si cap layer 214 which consists of Si of 5nm of thickness is carried out one by one.

[0068] Next, as shown in drawing 11 , the isolation insulating region 105 is formed by the technique in ordinary use, and it is the element formation field 121. It forms. The aforementioned isolation insulating region 105 is formed formation of a trench, and by embedding this trench by the oxide film.

[0069] Next, as shown in drawing 11 , while oxidizing thermally the front face of the aforementioned Si cap layer 214 and forming an oxide film, after forming a polysilicon contest film in piles, as it **********s and the polysilicon contest film and oxide film of a portion except a gate formation field are shown in drawing 12 , the gate oxide film 106 and the gate electrode 107 are formed.

[0070] Next, illustration is the aforementioned gate oxide film 106 like the case where it is the aforementioned operation form 1 although not carried out. And after forming a side attachment wall (sidewall) 122 in the both-sides side of the gate electrode 107, The diffusion field 108 which constitutes a source field and a drain field from a method in ordinary use by the self aryne using a side attachment

wall 122 is formed. Subsequently, the layer insulation film 109 is formed, a contact hole is broken, the metal wiring 111 is formed in the aforementioned contact hole portion by carrying out the vacuum evaporationo of the metal membranes, such as aluminum, and carrying out patterning, and an n type modulation dope type field effect transistor as shown in drawing 8 is formed. The aforementioned diffusion field 108 is formed so that it may reach by Fukashi in the middle of the distortion Si channel layer 104.

[0071] Moreover, in the ion implantation in formation of the aforementioned diffusion field 108, if an III group element is poured in, a p-channel type modulation dope type field effect transistor can be manufactured.

[0072] Also in the modulation dope type field effect transistor by this operation form 3, flattening becomes good by thin shape-ization of the SiGe distortion impression layer 102, the distortion Si channel layer 104 formed on the SiGe distortion impression layer 102 can also be made thin below the ** (3-2x) nm grade of 10, the fall of the mobility by reduction of punch-through current and transition generating into a channel layer can be prevented, and improvement in the speed of a field effect transistor and highly efficient-ization can be attained.

[0073] Moreover, thin-shape-izing of the distortion Si channel layer 104 by flattening of the SiGe distortion impression layer 102 to micro processing becomes possible, and high integration can be attained.

[0074] Moreover, by thin shape-ization of the SiGe distortion impression layer 102 and the distortion Si channel layer 104, shortening of film formation time can be aimed at and it will have the effect of being able to attain reduction of the manufacturing cost of a semiconductor device.

[0075] also in this operation form 3, reduction of the stray capacity of the field effect transistor of especially more a modulation dope type which adopts the technology which forms SiO2 insulating layer 103 so that the upper surface of SiO2 insulating layer 103 may be in agreement with the undersurface of the SiGe distortion impression layer 102 can be attained

[0076] Although invention made by this invention person above explained concretely based on an operation form, this invention is not limited to the above-mentioned operation form, and the same effect as the aforementioned example is acquired also by the case of the semiconductor device which it could not be overemphasized that it can change variously in the range which does not deviate from the summary, for example, formed other mixed-crystal semiconductor layers, such as GaAs, as a distortion impression layer 102 which forms on an Si substrate 101.

[0077] Although the above explanation explained the case where invention mainly made by this invention person was applied to the manufacturing technology of the field effect transistor which is a field of the invention used as the background, it is not limited to it.

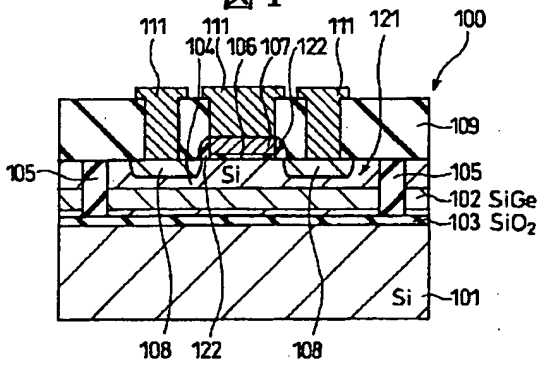
[0078] this invention is applicable to manufacture of the semiconductor device which has active elements, such as a transistor and diode, at least.

[Translation done.]

DRAWINGS

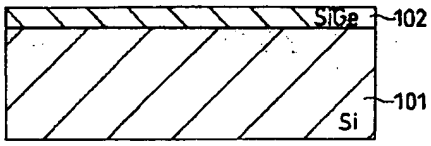
[Drawing 1]

図 1



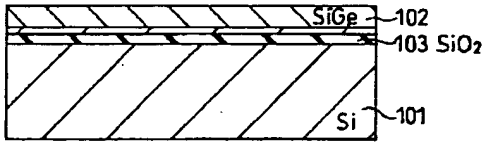
[Drawing 2]

図 2



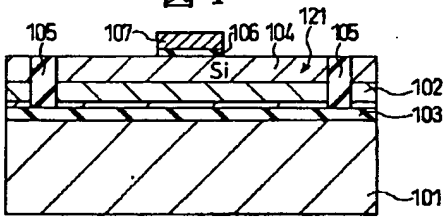
[Drawing 3]

図 3



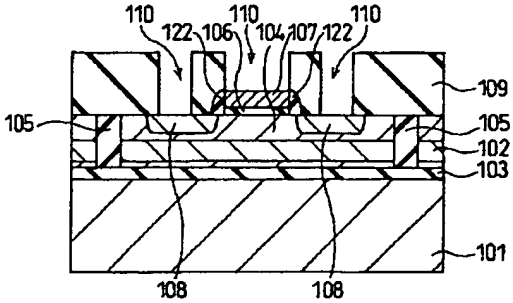
[Drawing 4]

図 4



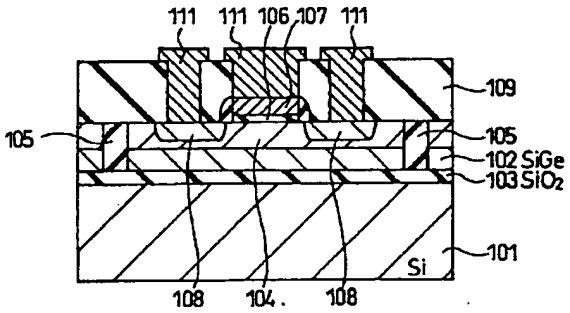
[Drawing 5]

図 5



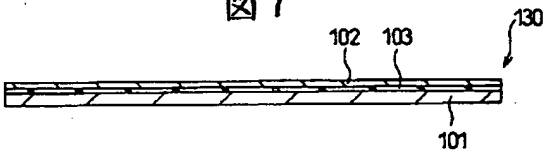
[Drawing 6]

図 6



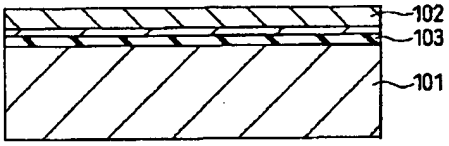
[Drawing 7]

図 7



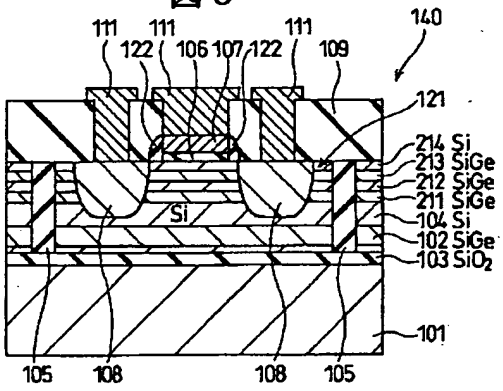
[Drawing 9]

図 9



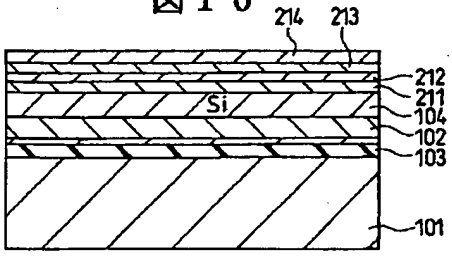
[Drawing 8]

図 8



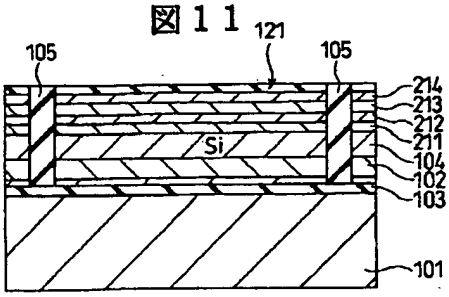
[Drawing 10]

図 1 0



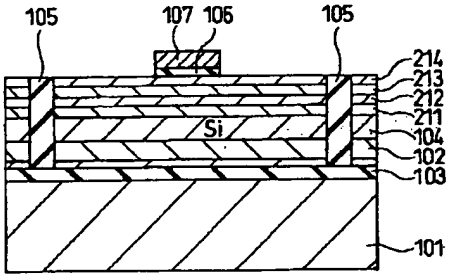
[Drawing 11]

図 1 1



[Drawing 12]

図 1 2



[Translation done.]

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☒ FADED TEXT OR DRAWING
- ☒ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.